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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,498	02/28/2002	David Finlay Taylor	4481-045	7479

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EXAMINER	
AGHDAM, FRESHTEH N	
ART UNIT	**PAPER NUMBER**
2631	

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DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,498	TAYLOR ET AL.	
	Examiner	Art Unit	
	Freshteh N. Aghdam	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 3 and 18 are objected to because of the following informalities:

As to claim 3, at page 12, line 20 the cited step "(e)" lacks antecedent basis.

As to claim 18, the recited measuring parameters should be defined in the claim as to prevent definiteness.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 3, 6, 7, 9-19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts et al, and further in view of Blazo (US 5,754,437).

As to claims 1 and 20, Roberts et al teach a method for reducing timing jitter in a receiver comprising sampling and digitizing the recovered clock signal to produce sample values (means 75); processing the digitized samples with reference to a local digital reference signal (i.e. e^jwt) to produce digital baseband frequency in-phase and quadrature components by (means 74); processing the baseband signal to extract

digital phase information of the signal (means 78); and processing the digital phase information to determine a parameter of the electronic system (i.e. timing jitter) see (Fig. 8; Col. 9, Lines 9-20 and 44-48). Roberts et al do not disclose recovering a clock signal from an input signal received from the electronic system. Blazo teaches a phase measurement apparatus and method wherein the input signal is clock recovered (Fig. 4A, means 70; Col. 8, Lines 63-67). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Blazo with Roberts et al in order to preserves the jitter on the incoming data transitions up to at least a frequency required by the applicable standard (Col. 8, Lines 65-67).

As to claim 2, the use of down converter is taught see (Fig 7, means 34) of Roberts et al. One of ordinary skill in the art would clearly recognize that it is well known in the art to use a digital down converter IC of a type suitable for digital radio receiver implementations.

As to claim 3, one of ordinary skill in the art would clearly recognize that it is a design choice to implement steps (d) and (f) in a single programmable digital signal processor chip.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts et al and Blazo, further in view of Hoffman et al (US 6,151,076).

As to claims 4 and 5, Roberts et al and Blazo teach all the subject matters claimed above, except for the network further comprises the step of frequency dividing the recovered clock signal prior to the sampling step. Hoffman et al, in the same field of endeavor, teach frequency dividing of the sampled clock signals in order to lock the

frequency of the digital clock signal for sampling while measuring the recovered clock signals of different frequencies (Fig. 1 and 3; Col. 1, Lines 10-14 and 65-67; Col. 2, Lines 1-12). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Hoffman et al with Roberts et al and Blazo in order to manage the phase jitter presented in the signal (Abstract; Col. 1, Lines 65-67).

As to claim 6, Roberts et al teach basebanding the digitized signal into in-phase and quadrature components and mixing the signal with the respective reference signal (e^jwt) derived from the result of the filter (Fig. 7, means 33; Fig. 8, means 71; Col. 9, Lines 45-49).

As to claim 7, Roberts et al teach processing the baseband signal to extract the phase information (means 78) further comprising the step of filtering and decimating the baseband signal (means 91 and 93) see (Fig. 8; Col. 9, Lines 43 and 44; Col. 10, Lines 24-29).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts et al and Blazo, further in view of Okubo et al (US 6,097,766).

As to claim 8, Roberts et al and Blazo teach all the subject matters as recited in claim 1. Okubo et al, in the same field of endeavor, teach extracting phase information comprises applying an inverse tangent function to the sampled baseband signal (Fig. 1; Col. 11, Lines 17-20). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Okubo et al with Roberts et al and Blazo in order to produce baseband phase data (Col. 11, Lines 17-20).

As to claim 9, Roberts et al teach controlling the phase of the local digital clock signal (means 77) in response to the extracted phase information outputted from (means 78) as part of a phase locked loop (Fig. 8; means 77, 78, and 79).

As to claim 10, Blazo further teaches processing the extracted phase information into clock jitter data by digitally filtering the phase information of the PLL (i.e. Phase Locked Loop) see (Fig. 4A and B, means 44, 36, 78, and 80; Col. 5, Lines 53-65; Col. 6, Lines 41-46; Col. 8, Lines 39-58). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Blazo with Roberts et al in order to perform the jitter and wander measurement over a wide range independent of loop bandwidth of the phase locked loop (Col. 5, Lines 3-5).

As to claim 11, Blazo further teaches filtering comprises high pass digital filtering of the phase information (Fig. 4B, means 80). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Blazo with Roberts et al in order to perform the jitter and wander measurement over a wide range independent of loop bandwidth of the phase locked loop (Col. 5, Lines 3-5).

As to claim 12, Blazo further teaches filtering comprises a low passs digital filtering stage additional to that in the phase locked loop (Fig. 4B, means 78). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Blazo with Roberts et al in order to perform the jitter and wander measurement over a wide range independent of loop bandwidth of the phase locked loop (Col. 5, Lines 3-5).

As to claim 13, Blazo further teaches the local digital reference signal is an externally sourced timing signal independent of the received signal (Fig. 4A, MEANS

34; Col. 3, Lines 51-53; Col. 7, Lines 44-49). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Blazo with Roberts et al in order to support the jitter and wander measurements (Col. 7, Lines 44-46).

As to claims 14 and 16, Blazo teaches processing the extracted phase information into the clock time interval error data by filtering the phase information wherein the resultant time interval error data is further processed to derive wander data (Fig. 4B, means 82; Col. 14, Lines 58-67; Col. 13, Lines 44-50; Col. 15, Lines 1-4). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Blazo with Roberts et al in order to perform the jitter and wander measurement over a wide range independent of loop bandwidth of the phase locked loop (Col. 5, Lines 3-5).

As to claim 15, Blazo further teaches filtering comprises a low pass digital filtering stage additional to that in the phase locked loop (Fig. 4B, means 78 and 82). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Blazo with Roberts et al in order to perform the jitter and wander measurement over a wide range independent of loop bandwidth of the phase locked loop (Col. 5, Lines 3-5).

As to claim 17, Blazo et al further teaches implementing the method of jitter and wander measurements in a form of hardware switchable between phase locked and independent reference signals responsive to the desired measurement (Fig. 4 A and B; Col. 7, Lines 44-64; Col. Col. 9, Lines 1-4 and 45-47). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Blazo with Roberts

et al in order to perform the jitter and wander measurement over a wide range independent of loop bandwidth of the phase locked loop (Col. 5, Lines 3-5).

As to claim 18, Blazo further teaches using RMS and PK-PK (i.e. Peak to Peak) as defined by the ITU standard (Fig. 4B).

As to claim 19, one of ordinary skill in the art would clearly recognize that it is a design choice to implement the recited measurement tasks within a single signal processor.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.Takao et al (US 5,920,220), Fujimura et al (US 6,415,004), Doh et al (US 6,684,033).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freshteh N. Aghdam whose telephone number is (571) 272-6037. The examiner can normally be reached on Monday through Friday 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Freshteh Aghdam

May 10, 2005

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